

NLASB3157

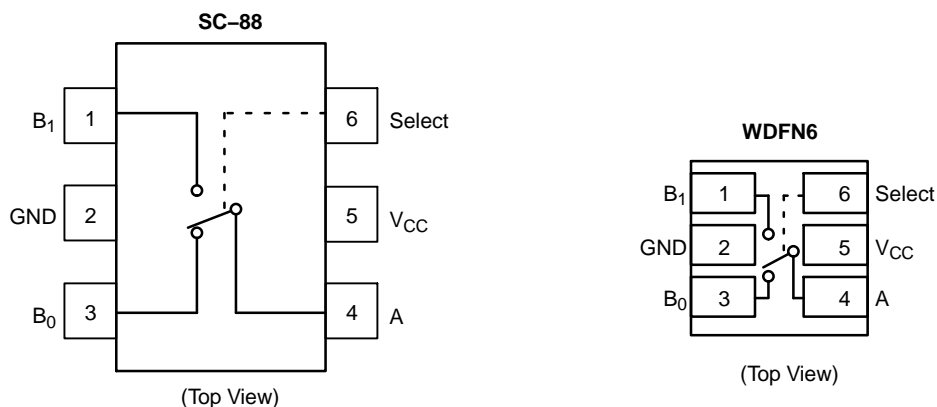


Figure 1. Pin Assignment & Logic Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
DC Switch Voltage (Note 1)	V_{IS}	-0.5 to $V_{CC} + 0.5$	V
DC Input Voltage (Note 1)	V_{IN}	-0.5 to + 7.0	V
DC Input Diode Current @ $V_{IN} < 0$ V	I_{IK}	-50	mA
DC Input / Output Current	I_{OUT}	128	mA
DC V_{CC} or Ground Current	I_{CC}/I_{GND}	+100	mA
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature Under Bias	T_J	150	°C
Junction Lead Temperature (Soldering, 10 Seconds)	T_L	260	°C
Power Dissipation @ +85°C	P_D	180	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

RECOMMENDED OPERATING CONDITIONS (Note 2)

Characteristic	Symbol	Min	Max	Unit
Supply Voltage Operating	V_{CC}	1.65	5.5	V
Select Input Voltage	V_{IN}	0	5.5	V
Switch Input Voltage	V_{IS}	0	V_{CC}	V
Output Voltage	V_{OUT}	0	V_{CC}	V
Operating Temperature	T_A	-55	+125	°C
Input Rise and Fall Time Control Input $V_{CC} = 2.3$ V–3.6 V Control Input $V_{CC} = 4.5$ V–5.5 V	t_r, t_f	0	10 5.0	ns/V
Thermal Resistance	J_A	-	350	°C/W

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. Select input must be held HIGH or LOW, it must not float.

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DC ELECTRICAL CHARACTERISTICS – NLASB3157

Symbol	Parameter	Test Conditions	V _{CC} (V)	T _A = +25°C			T _A = -40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	HIGH Level Input Voltage		1.65–1.95 2.3–5.5				0.75 V _{CC} 0.7 V _{CC}		V
V _{IL}	LOW Level Input Voltage		1.65–1.95 2.3–5.5					0.25 V _{CC} 0.3 V _{CC}	V
I _{IN}	Input Leakage Current	0 ≤ V _{IN} ≤ 5.5 V	0–5.5		±0.05	±0.1		±1	A
I _{OFF}	OFF State Leakage Current	0 ≤ A, B ≤ V _{CC}	1.65–5.5		±0.05	±0.1		±1	A
R _{ON}	Switch On Resistance (Note 3)	V _{IN} = 0 V, I _O = 30 mA	4.5		3.0			7.0	
		V _{IN} = 2.4 V, I _O = -30 mA			5.0			12	
		V _{IN} = 4.5 V, I _O = -30 mA			7.0			15	
		V _{IN} = 0 V, I _O = 24 mA	3.0		4.0			9.0	
		V _{IN} = 3 V, I _O = -24 mA			10			20	
		V _{IN} = 0 V, I _O = 8 mA	2.3		5.0			12	
		V _{IN} = 2.3 V, I _O = -8 mA			13			30	
		V _{IN} = 0 V, I _O = 4 mA	1.65		6.5			20	
		V _{IN} = 1.65 V, I _O = -4 mA			17			50	
I _{CC}	Quiescent Supply Current All Channels ON or OFF	V _{IN} = V _{CC} or GND I _{OUT} = 0	5.5			1.0		10	A
	Analog Signal Range		V _{CC}	0		V _{CC}	0	V _{CC}	V
R _{RANGE}	On Resistance Over Signal Range (Note 3) (Note 7)	I _A = -30 mA, 0 ≤ V _{Bn} ≤ V _{CC}	4.5					25	
		I _A = -24 mA, 0 ≤ V _{Bn} ≤ V _{CC}	3.0					50	
		I _A = -8 mA, 0 ≤ V _{Bn} ≤ V _{CC}	2.3					100	
		I _A = -4 mA, 0 ≤ V _{Bn} ≤ V _{CC}	1.65					300	
R _{ON}	On Resistance Match Between Channels (Note 3) (Note 4) (Note 5)	I _A = -30 mA, V _{Bn} = 3.15	4.5		0.15				
		I _A = -24 mA, V _{Bn} = 2.1	3.0		0.2				
		I _A = -8 mA, V _{Bn} = 1.6	2.3		0.5				
		I _A = -4 mA, V _{Bn} = 1.15	1.65		0.5				
R _{flat}	On Resistance Flatness (Note 3) (Note 4) (Note 6)	I _A = -30 mA, 0 ≤ V _{Bn} ≤ V _{CC}	5.0		6.0				
		I _A = -24 mA, 0 ≤ V _{Bn} ≤ V _{CC}	3.3		12				
		I _A = -8 mA, 0 ≤ V _{Bn} ≤ V _{CC}	2.5		28				
		I _A = -4 mA, 0 ≤ V _{Bn} ≤ V _{CC}	1.8		125				

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).
- Parameter is characterized but not tested in production.
- R_{ON} = R_{ON} max – R_{ON} min measured at identical V_{CC}, temperature and voltage levels.
- Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.
- Guaranteed by Design.

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AC ELECTRICAL CHARACTERISTICS – NLASB3157

Symbol	Parameter	Test Conditions	V _{CC} (V)	T _A = +25°C	T _A = -40°C to +85°C	Unit
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Figure9(e)-9.1(s)-9.1(t)25

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APPENDIX A

DC ELECTRICAL EXTENDED AUTOMOTIVE TEMPERATURE RANGE CHARACTERISTICS – NLVASB3157

Symbol	Parameter	Test Conditions	V _{CC} (V)	T _A = +25°C			T _A = -55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	HIGH Level Input Voltage		1.65–1.95 2.3–5.5				0.75 V _{CC} 0.7 V _{CC}		V
V _{IL}	LOW Level Input Voltage		1.65–1.95 2.3–5.5					0.25 V _{CC} 0.3 V _{CC}	V
I _{IN}	Input Leakage Current	0 ≤ V _{IN} ≤ 5.5 V	0–5.5		±0.05	±0.1		±1	A
I _{OFF}	OFF State Leakage Current	0 ≤ A, B ≤ V _{CC}	1.65–5.5		±0.05	±0.1		±1	A
R _{ON}	Switch On Resistance (Note 12)	V _{IN} = 0 V, I _O = 30 mA	4.5		3.0			8.5	
		V _{IN} = 2.4 V, I _O = -30 mA			5.0			13.0	
		V _{IN} = 4.5 V, I _O = -30 mA			7.0			15.0	
		V _{IN} = 0 V, I _O = 24 mA	3.0		4.0			11	
		V _{IN} = 3 V, I _O = -24 mA			10			20	
		V _{IN} = 0 V, I _O = 8 mA	2.3		5.0			12	
		V _{IN} = 2.3 V, I _O = -8 mA			13			30	
		V _{IN} = 0 V, I _O = 4 mA	1.65		6.5			20	
		V _{IN} = 1.65 V, I _O = -4 mA			17			50	
I _{CC}	Quiescent Supply Current All Channels ON or OFF	V _{IN} = V _{CC} or GND I _{OUT} = 0	5.5			1.0		10	A
	Analog Signal Range		V _{CC}	0		V _{CC}	0	V _{CC}	V
R _{RANGE}	On Resistance Over Signal Range (Note 12) (Note 14)	I _A = -30 mA, 0 ≤ V _{Bn} ≤ V _{CC}	4.5					25	
		I _A = -24 mA, 0 ≤ V _{Bn} ≤ V _{CC}						50	
		I _A = -8 mA, 0 ≤ V _{Bn} ≤ V _{CC}	3.0					100	
		I _A = -4 mA, 0 ≤ V _{Bn} ≤ V _{CC}	2.3					300	
			1.65						

12. Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).

13. Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.

14. Guaranteed by Design.

* For ΔR_{ON}, R_{FLAT}, Q, OIRR, Xtalk, BW, THD, and CIN see -40°C to 85°C section.

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APPENDIX A

AC ELECTRICAL EXTENDED AUTOMOTIVE TEMPERATURE RANGE CHARACTERISTICS – NLVASB3157

Symbol	Parameter	Test Conditions	V _{CC} (V)	T _A = +25°C			T _A = -55°C to +125°C		Unit	Figure Number
				Min	Typ	Max	Min	Max		
t _{PHL} t _{PLH}	Propagation Delay Bus to Bus (Note 16)	V _I = OPEN	1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5					1.2 0.8 0.3	ns	Figures 2, 3
t _{PZL} t _{PZH}	Output Enable Time Turn On Time (A to B _n)	V _I = 2 × V _{CC} for t _{PZL} V _I = 0 V for t _{PZH}	1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5			23 13 6.9 5.2	7.0 3.5 2.5 1.7	24 14 9.0 7.0	ns	Figures 2, 3
t _{PLZ} t _{PHZ}	Output Disable Time Turn Off Time (A Port to B Port)	V _I = 2 × V _{CC} for t _{PLZ} V _I = 0 V for t _{PHZ}	1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5			12.5 7.0 5.0 3.5	3.0 2.0 1.5 0.8	13 7.5 6.5 5.0	ns	Figures 2, 3
t _{B-M}	Break Before Make Time (Note 15)		1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5				0.5 0.5 0.5 0.5		ns	Figure 4

15. Guaranteed by Design.

16. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

* For ΔR_{ON}, R_{FLAT}, Q, OIRR, Xtalk, BW, THD, and CIN see -40°C to 85°C section.

AC LOADING AND WAVEFORMS

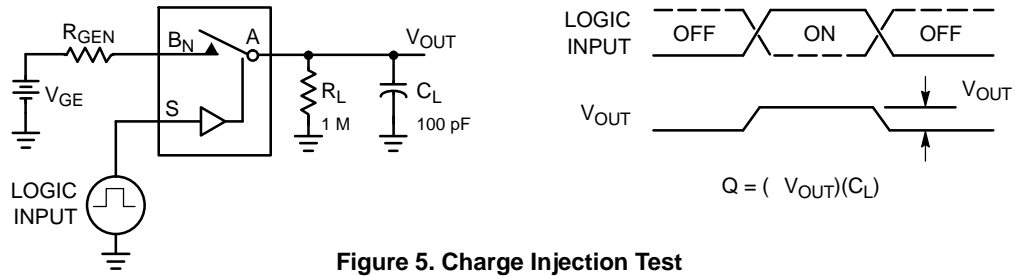


Figure 5. Charge Injection Test

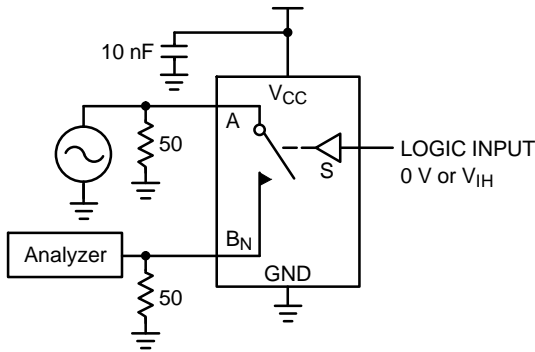


Figure 6. Off Isolation

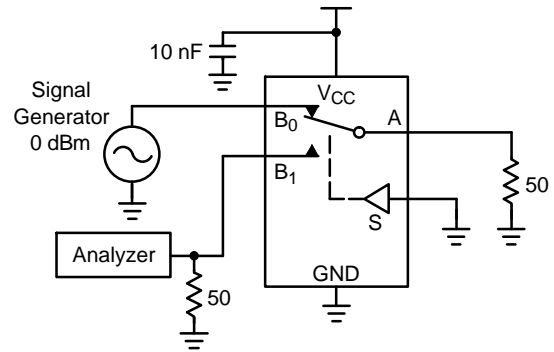


Figure 7. Crosstalk

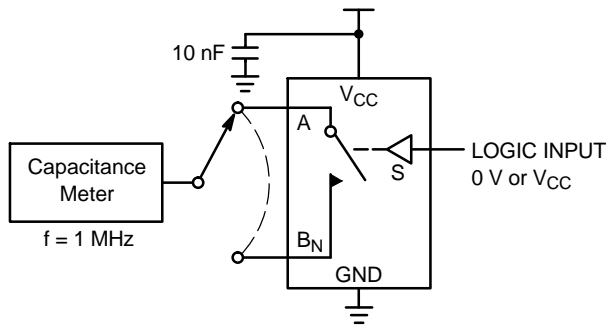


Figure 8. Channel Off Capacitance

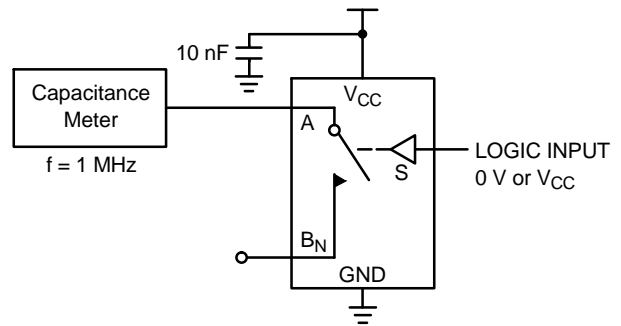


Figure 9. Channel On Capacitance

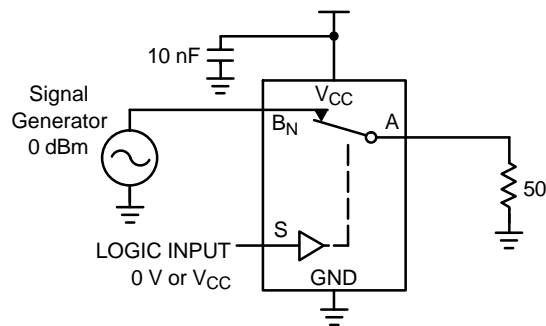
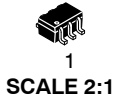
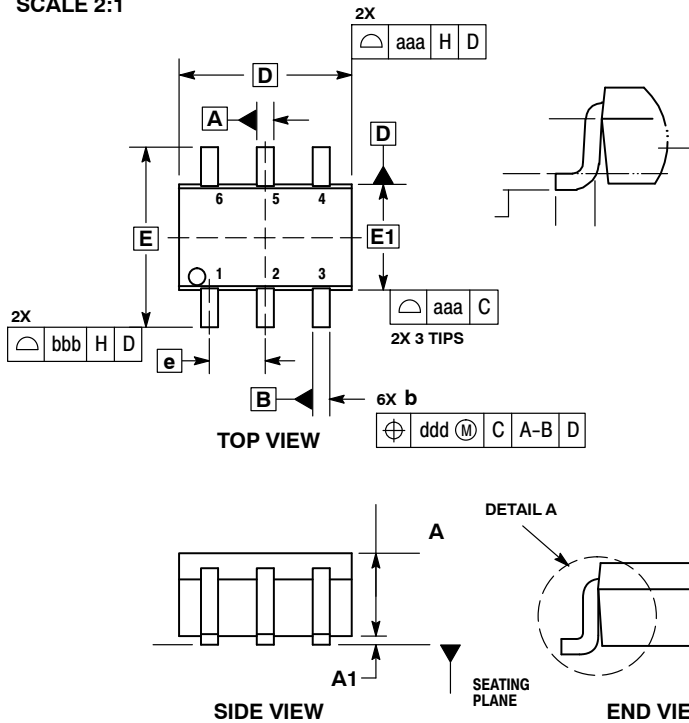


Figure 10. Bandwidth



SC-88/SC70-6/SOT-363
CASE 419B-02
ISSUE Y

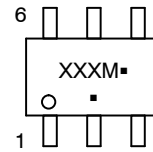
DATE 11 DEC 2012



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
 4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
 5. DATUMS A AND B ARE DETERMINED AT DATUM H.
 6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
 7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

GENERIC MARKING DIAGRAM*

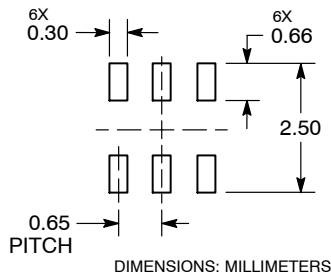


- XXX = Specific Device Code
- M = Date Code*
- = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SC-88/SC70-6/SOT-363
CASE 419B-02
ISSUE Y

DATE 11 DEC 2012

STYLE 1: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	STYLE 2: CANCELLED	STYLE 3: CANCELLED	STYLE 4: PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE	STYLE 5: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 6: PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2
STYLE 7: PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2	STYLE 8: CANCELLED	STYLE 9: PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2	STYLE 10: PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2	STYLE 11: PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2	STYLE 12: PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2
STYLE 13: PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 14: PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC	STYLE 15: PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1	STYLE 16: PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1	STYLE 17: PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1	STYLE 18: PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1
STYLE 19: PIN 1. IOUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF	STYLE 20: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR	STYLE 21: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1	STYLE 22: PIN 1. D1 (i) 2. GND 3. D2 (i) 4. D2 (c) 5. VBUS 6. D1 (c)	STYLE 23: PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C	STYLE 24: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
STYLE 25: PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1	STYLE 26: PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1	STYLE 27: PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2	STYLE 28: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	STYLE 29: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE	STYLE 30: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

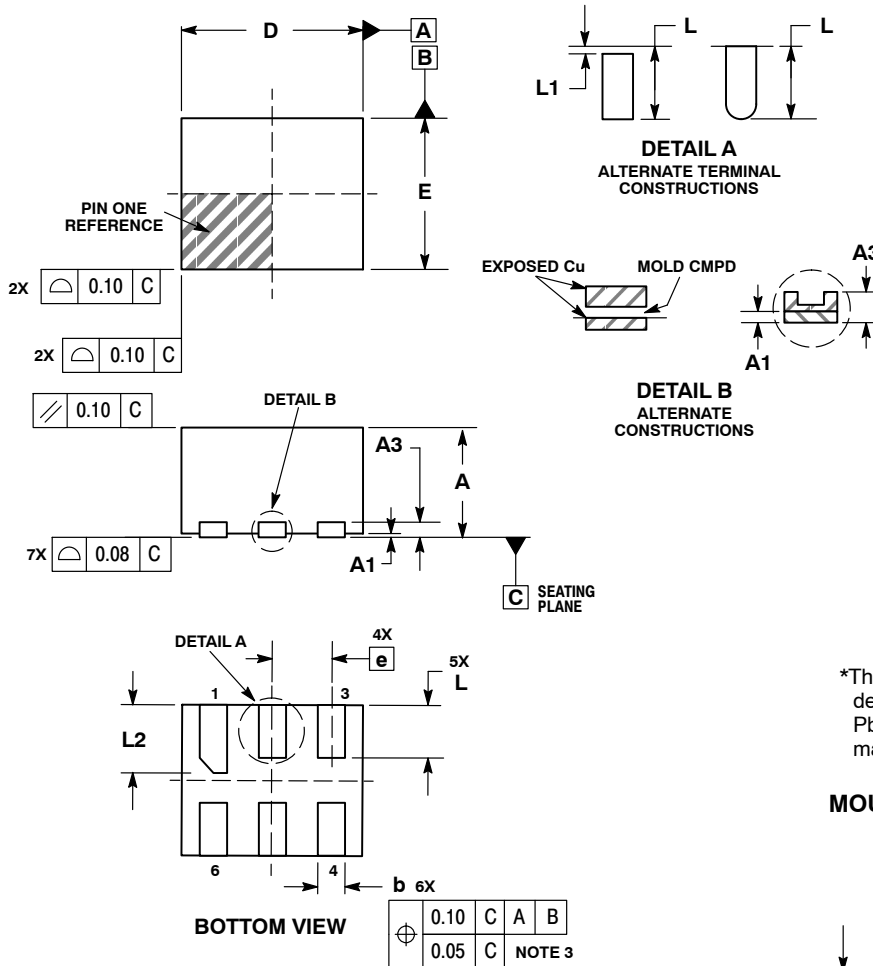


WDFN6 1.2x1.0, 0.4P CASE 506AS ISSUE D

DATE 27 AUG 2013



SCALE 4:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	1.20 BSC	
E	1.00 BSC	
e	0.40 BSC	
L	0.30	0.40
L1	0.00	0.15
L2	0.40	0.50

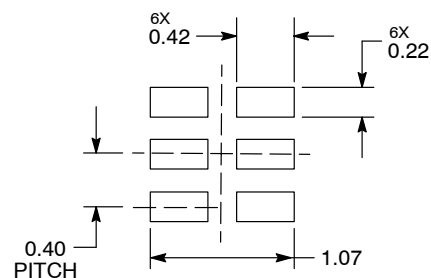
GENERIC MARKING DIAGRAM*



X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

- STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

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